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FINAL YEAR PROJECTS

IEEE PROJECTS 2016 – 2017

VLSI PROJECTS

S.NO	PROJECT CODE	TITLE OF THE PAPER	YEAR
1	VL1601	A Fully Digital Front-End Architecture for ECG Acquisition System With 0.5 V Supply	2016
2	VL1602	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	2016
3	VL1603	RF Power Gating: A Low-Power Technique for Adaptive Radios	2016
4	VL1604	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia Capacitance Tomography	2016
5	VL1605	A New Parallel VLSI Architecture for Real-Time Electrical	2016
6	VL1606	Low-Power FPGA Design Using Memoization-Based Approximate Computing	2016
7	VL1607	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	2016
8	VL1608	A High-Speed FPGA Implementation of an RSD-Based ECC Processor	2016
9	VL1609	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2016
10	VL1610	A 0.52/1 V Fast Lock-in ADPLL for Supporting Dynamic Voltage and Frequency Scaling	2016
11	VL1611	Code Compression for Embedded Systems Using Separated Dictionaries	2016
12	VL1612	A Dynamically Reconfigurable Multi-ASIP Architecture for Multi-standard and Multimode Turbo Decoding	2016
13	VL1613	Design and Implementation of High-Speed All-Pass Transformation-Based Variable Digital Filters by Breaking the Dependence of Operating Frequency on Filter Order	2016
14	VL1614	A Mixed-Decimation MDF Architecture for Radix-2K Parallel FFT	2016
15	VL1615	Algorithm and Architecture of Configurable Joint Detection and Decoding for	2016

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		MIMO Wireless Communications With Convolution Codes	
16	VL1616	One-Cycle Correction of Timing Errors in Pipelines With Standard Clocked Elements	2016
17	VL1617	Hardware and Energy-Efficient Stochastic LU Decomposition Scheme for MIMO Receivers	2016
18	VL1618	Hybrid LUT/Multiplexer FPGA Logic Architectures	2016
19	VL1619	A 520k (18 900, 17 010) Array Dispersion LDPC Decoder Architectures for NAND-Flash Memory	2016
20	VL1620	Implementing Minimum-Energy-Point Systems With Adaptive Logic	2016
21	VL1621	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2m)	2016
22	VL1622	High-Performance NB-LDPC Decoder With Reduction of Message Exchange	2016
23	VL1623	LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter	2016
24	VL1624	Graph-Based Transistor Network Generation Method for Supergate Design	2016
25	VL1625	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2016
26	VL1626	A Cellular Network Architecture With Polynomial Weight Functions	2016
27	VL1627	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2016
28	VL1628	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	2016
29	VL1629	Exploiting Intracell Bit-Error Characteristics to Improve Min-Sum LDPC Decoding for MLC NAND Flash-Based Storage in Mobile Device	2016
30	VL1630	Unequal-Error-Protection Error Correction Codes for the	2016
31	VL1631	A High Throughput List Decoder Architecture for Polar Codes	2016
32	VL1632	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	2016
33	VL1633	Design and FPGA Implementation of a Reconfigurable 1024- Channel Channelization Architecture for SDR Application	2016
34	VL1634	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	2016
35	VL1635	A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing	2016
36	VL1636	A New Binary-Halved Clustering Method and ERT Processor for ASSR System	2016
37	VL1637	The VLSI Architecture of a Highly Efficient De-blocking Filter for HEVC Systems	2016
38	VL1638	Low-Power System for Detection of Symptomatic Patterns in Audio Biological Signals	2016
39	VL1639	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	2016

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40	VL1640	Source Code Error Detection in High-Level Synthesis Functional Verification	2016
41	VL1641	A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell	2016
42	VL1642	OTA-Based Logarithmic Circuit for Arbitrary Input Signal and Its Application	2016
43	VL1643	A Robust Energy/Area-Efficient Forwarded-Clock Receiver With All-Digital Clock and Data Recovery in 28-nm CMOS for High-Density Interconnects	2016
44	VL1644	Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation	2016
45	VL1645	A 0.1-3.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS	2016
46	VL1646	A Low-Power Robust Easily Cascaded PentaMTJ-Based Combinational and Sequential Circuits	2016
47	VL1647	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	2016
48	VL1648	Low-Energy Power-ON-Reset Circuit for Dual Supply SRAM	2016
49	VL1649	Frequency-Boost Jitter Reduction for Voltage-Controlled Ring Oscillators	2016
50	VL1650	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	2016